CLAIMS

1. A processing system for providing a distributed directory based coherence protocol incorporating prefetching buffers, comprising:

a memory hierarchy level having a coherence directory and associated directory data;

a plurality of prefetch address registers;

a plurality of memory blocks each associated with different directory data;

a plurality of buffers interconnected to said memory;

a plurality of processing elements, each said processing element interconnected to different buffers of said plurality of buffers;

means for requesting selected said memory blocks from said memory;

means associated with said memory, responsive to said means for requesting for delivery, in response to said requesting, for delivery of a corresponding memory block of said memory blocks, a corresponding set of said coherence directory data from said memory, to an associated element of said processing elements, further incorporating the value of prefetch address registers in said response; and

means for said processing elements for detecting said delivery of said memory block, if said memory block of said processing element is available for a particular access mode, and if not, performing coherence actions corresponding to said coherence directory data.

2. The system of Claim 1, where the processing elements are connected with said buffers connected to the memory via point to point links.

3. The system of Claim 1 where the process of incorporating the value of the prefetch address register is performed by including the value of at least one prefetch address register from said memory hierarchy level as field in said response.

4. The system of Claim 1 wherein the process of incorporating the value of the prefetch address register comprises a transmitted directory information modifier, indicating for the coherence directory information, the combined coherence information stored in the memory hierarchy level in the coherence directory entries and the prefetch address registers.

5. The system of Claim 1, wherein the response generated includes a plurality of memory blocks and their associated directory coherence entries.

6. The system of Claim 5, wherein the plurality of the memory blocks and the associated coherence directory data transmitted in the response are stored in a prefetch buffer, and an identifying address of said plurality of memory blocks is stored in at least one of the prefetch address register in said memory hierarchy level.

7. The system of Claim 6 wherein a prefetched plurality of memory blocks stored in a prefetch buffer are employed to provide memory data if said stored coherence directory data indicates compatible access modes for one of shared and both shared and exclusive memory access modes.

8. The system of claim 7 wherein an address stored in said prefetch register indicates that said memory block within

said indicated prefetch block may be used for one of shared and both shared and exclusive access.

9. The system of Claim 1 wherein said prefetch register further indicates the size of said prefetch request.

10. The system of Claim 1 wherein one said prefetch address register is associated with each said processing element, said prefetch address register automatically being updated to the value of the most recent said prefetch request.

11. The system of Claim 1 wherein a plurality of said prefetch address registers are associated with each said processing element corresponding to a plurality of said prefetch buffers in each said processing element, said processing element indicating which said prefetch register to update in correspondence to a specific said prefetch buffer being reloaded.

12. The system of Claim 1, wherein a protocol request is used to update at least one said coherence directory entry in response to satisfying a memory request from said prefetch buffer.

13. The system of Claim 1, wherein an optimized protocol request combines updates to at least one said coherence directory with a request for at least one said memory block and its associated said coherence directory entry.

14. A method implementing a distributed directory based coherence protocol supporting the presence of prefetch buffers, comprising:

requesting a memory block from a memory hierarchy level having a coherence directory, associated directory data, and prefetch address registers,

generating a response including memory data and coherence information,

updating directory information and indicating the address of a prefetched block in a prefetch address register,

receiving a response including memory data and coherence information from said memory hierarchy level,

a testing step to indicate whether received coherence information is compatible with required access mode,

a step of performing coherence actions if said test indicates one of incompatibility, and possible incompatibility,

a step of providing data which has been obtained to a requestor of memory data.

15. The method of Claim 14 wherein providing said coherence information provides separate coherence directory information and prefetch address information.

16. The method of Claim 15 wherein providing said coherence information provides merged coherence data, said merged coherence data having been obtained by combining the information contained in at least one coherence directory entry and at least one prefetch address register.

17. The method of Claim 14, wherein the method obtains a first data unit for processing in the processor core, and at least one additional data unit for storage in said prefetch buffer.

18. The method of Claim 16, wherein the requesting, generating, updating and receiving steps are skipped when a data item can be obtained from said prefetch buffer.

19. The method of Claim 16, wherein coherence actions are performed to obtain data, said first data item and coherence actions are suppressed for at least said additional data unit.

20. The method of Claim 19, wherein suppression is under the control of a prediction logic.

21. The method of Claim 14, wherein requests and responses are performed by sending and receiving data over logical point to point links.

22. The method of Claim 14 where at least one prefetch address register stores at least a prefetch address and a prefetch data length.

23. The method of Claim 12, where the step of performing coherence actions uses information about data location provided by at least one of data stored in the coherence directory and information about prefetch address register allocation to specific processing elements.

24. A computer program product for authenticating code in a computer system, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer code for providing a distributed directory based coherence protocol incorporating prefetch cache logic; and

computer code for ordering a memory block movement command having an associative coherence directory data movement command.

25. A directory-based coherence system with distributed directory management utilizing prefetch cache for providing data coherence in a computer system, including a computer program comprising:

computer code for requesting memory blocks from memory through requesting, acknowledging and delivery logic; and

computer code for ordering a memory block movement along with computer code for having an associative coherence directory data movement command.